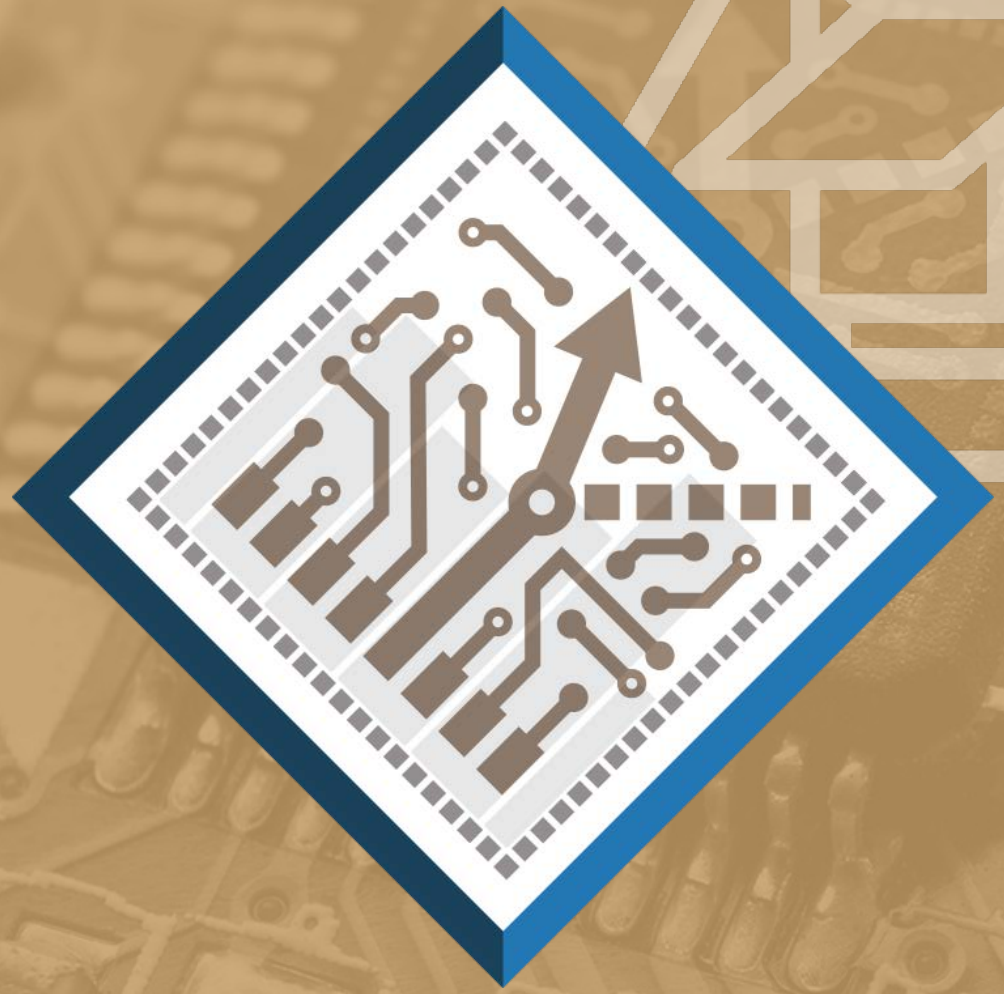
WADE SHEN

PROGRAM MANAGER
DARPA/I2O & MTO



SOFTWARE DEFINED HARDWARE (SDH)

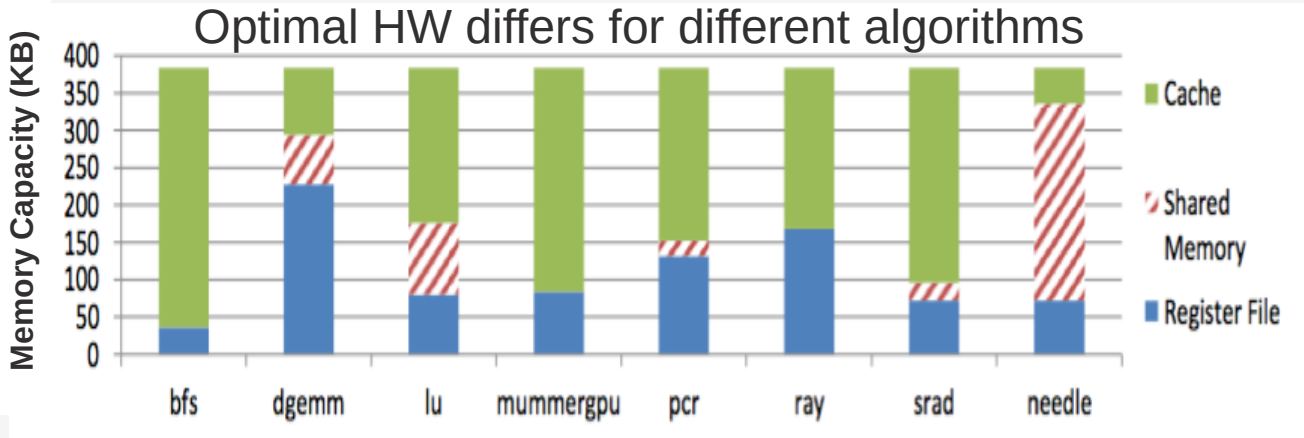
SDH

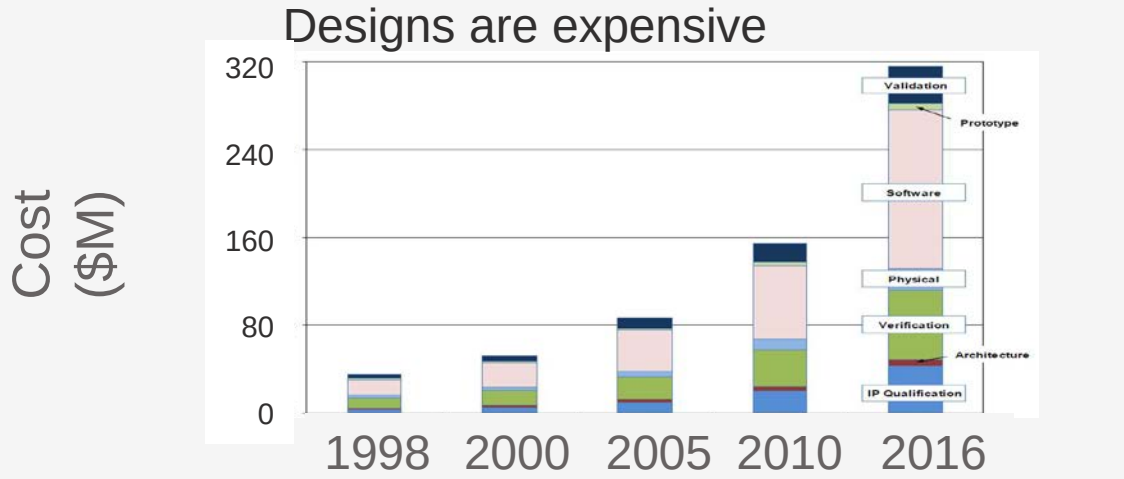
PROGRAM DESCRIPTION

Build runtime reconfigurable hardware and software that enables near ASIC performance (within 10x) without sacrificing programmability for data-intensive algorithms.

SDH Metrics and Targets (from BAA):

	vs. CPU	vs. ASIC	vs. ASIC (sparse math, search, graphs)	Programmability
Phase 1	100-300x better	within 50x	~1x	within 10x
Phase 2	100-300x better	within 10x	2x better	within 3x
Phase 3	500-1000x better	within 5x	8-10x better	~1x

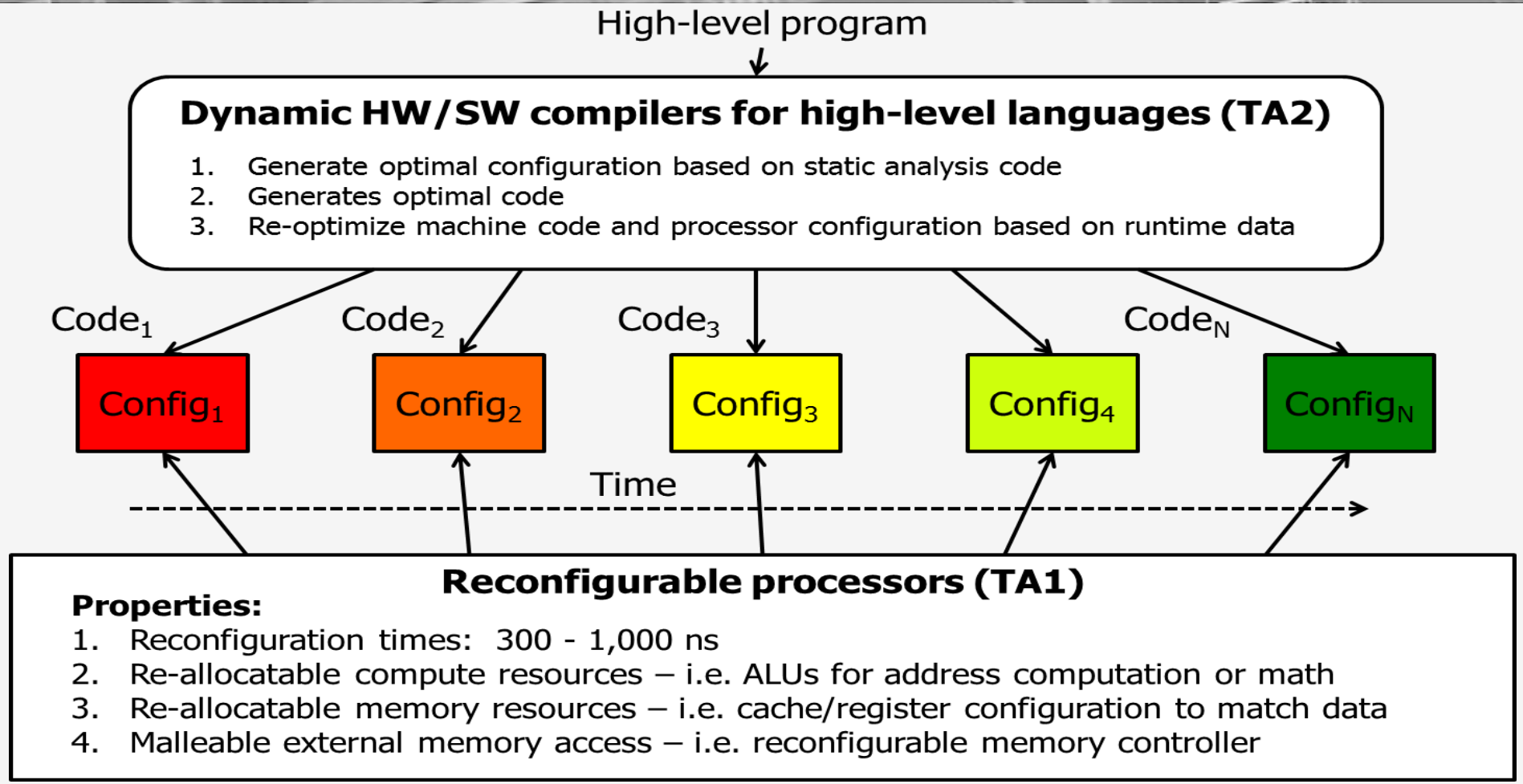




Today's specialization = expensive and inflexible designs

SDH

PROGRAM OVERVIEW



SDH

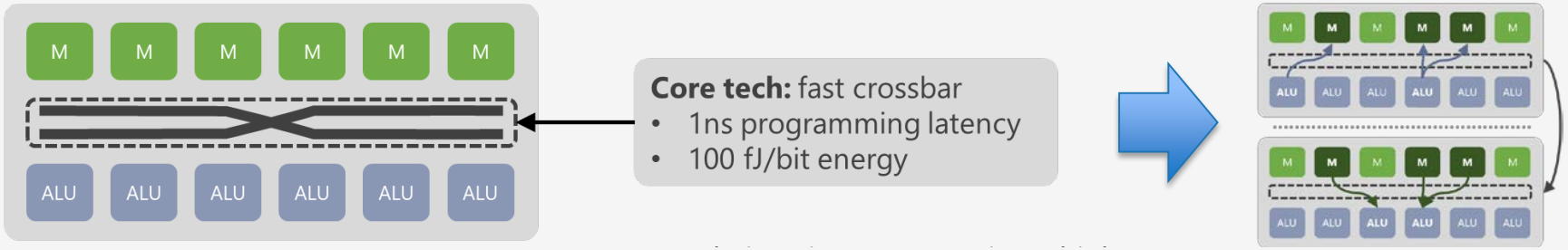
PROGRAM HIGHLIGHTS

Compute at and near memory: Princeton and Washington

Reduced data movement: lower power, lower latency; more efficient use of processor resources

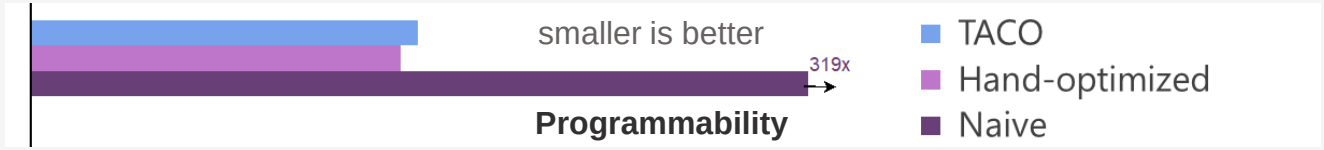
5x speed improvements + >10x power reduction for data intensive algorithms

Fast + efficient interconnect: Michigan

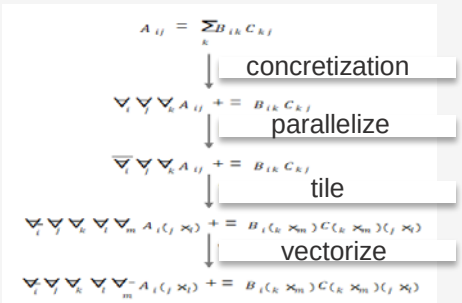


Reconfiguration based to match application and real time, dynamic data

Auto code generation for tensor math: NVIDIA/MIT



Hand-optimized = Code “Ninja” + 12 months

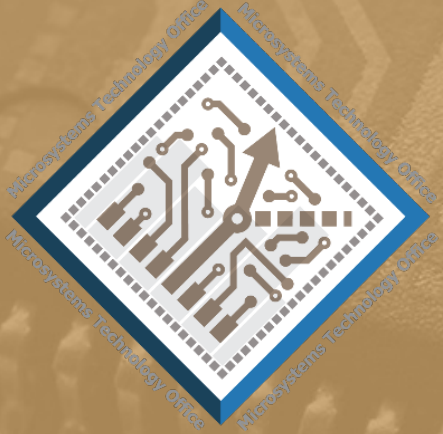


Tensor Algebra Compiler: TACO

PROGRAM ACRONYM

PERFORMERS

NVIDIA *PI: Stephen Keckler*	TA1: Reconfigurable processor architectures & TA2: Dynamic HW/SW compilers for high-level languages
Princeton University PI: Margaret Martonosi	TA1: Reconfigurable processor architectures & TA2: Dynamic HW/SW compilers for high-level languages
Stanford University *PI: Kunle Olukotun*	TA1: Reconfigurable processor architectures & TA2: Dynamic HW/SW compilers for high-level languages
University of Michigan *PI: Ronald Dreslinski*	TA1: Reconfigurable processor architectures & TA2: Dynamic HW/SW compilers for high-level languages
University of Washington *PI: Michael Taylor*	TA1: Reconfigurable processor architectures & TA2: Dynamic HW/SW compilers for high-level languages
Intel *PI: Josh Fryman*	TA1: Reconfigurable processor architectures
Qualcomm Intelligent Solutions, Inc. *PI: Shekhar Borkar*	TA1: Reconfigurable processor architectures
Georgia Tech *PI: Vivek Sarkar*	TA2: Dynamic HW/SW compilers for high-level languages
Systems & Technology Research *PI: Brad Gaynor*	TA2: Dynamic HW/SW compilers for high-level languages



ERI ELECTRONICS RESURGENCE INITIATIVE

SUMMIT

2019 | Detroit, MI | **July 15 - 17**