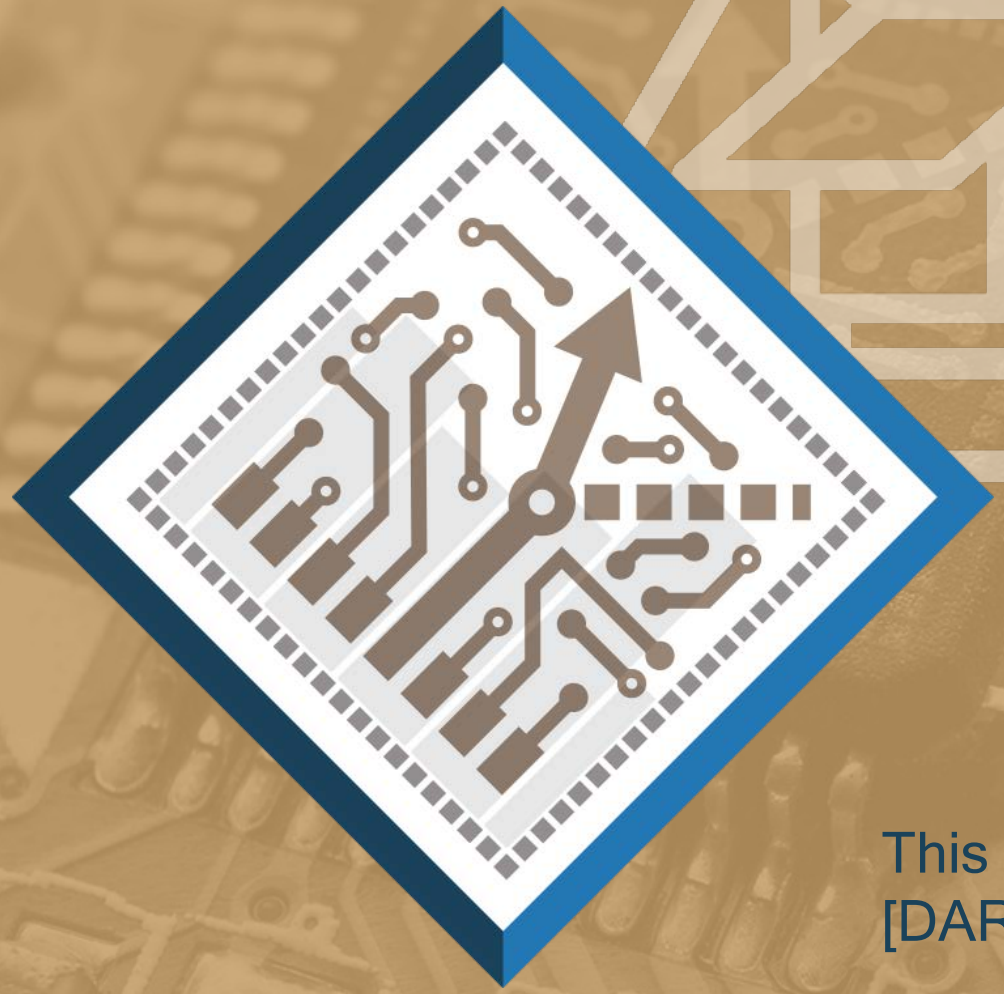
SERGEY SHUMARAYEV

DISTINGUISHED ARCHITECT
INTEL PSG CTO OFFICE



CHIPLET INTEGRATION DRIVES INNOVATION

This work is supported by the DARPA MTO office [DARPA CHIPS Contract Number: HR00111790020].

SYNCHRONIZED CO-ARCHITECTURE IS ESSENTIAL

“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected[1].”

Gordon E. Moore

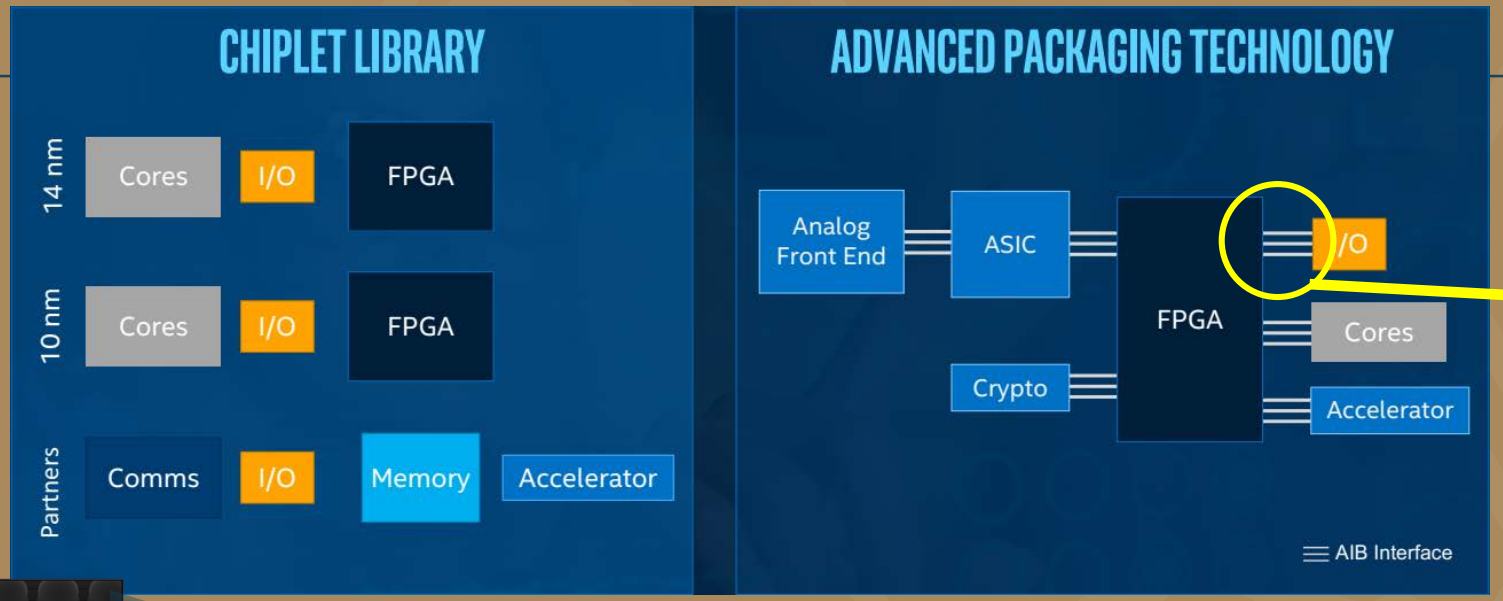
Connect chips and chiplets in a package to match or exceed the functionality of a monolithic SOC

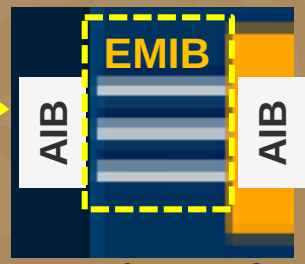
High density, low cost interconnect with high bandwidth at low power is essential

[1]Moore’s Law paper

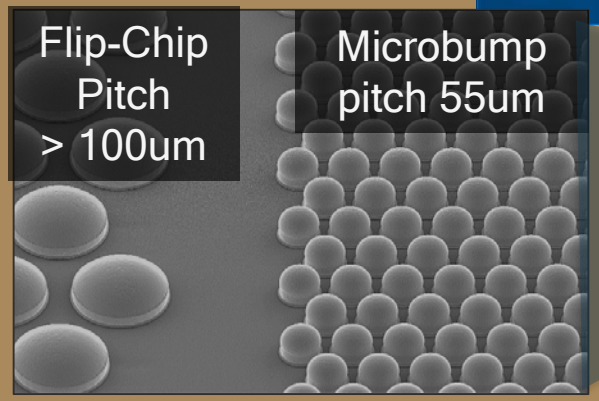
INNOVATION WITH PARTNERS

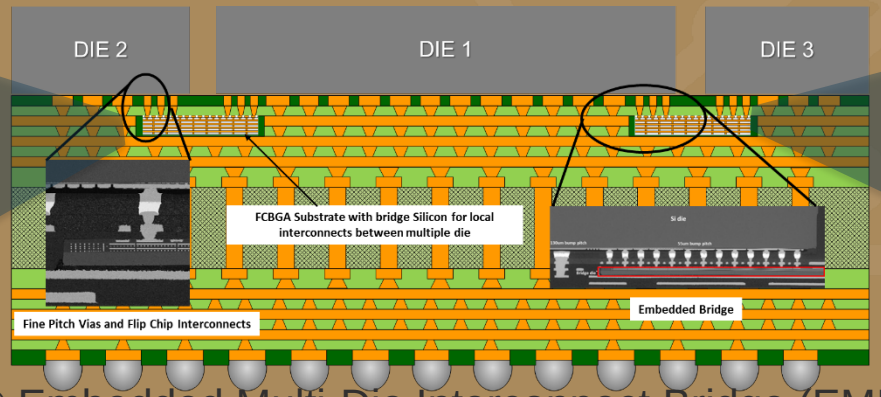
ADC/DAC
Machine Learning
Memory
Processors
Adjacent IP
…Your Ideas

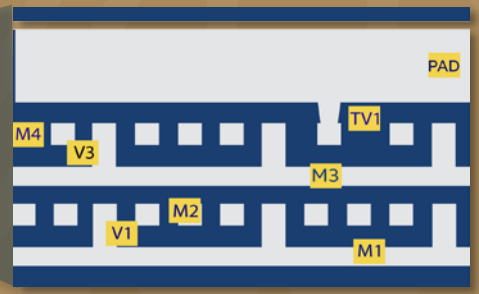




Advanced Interface Bus (AIB)



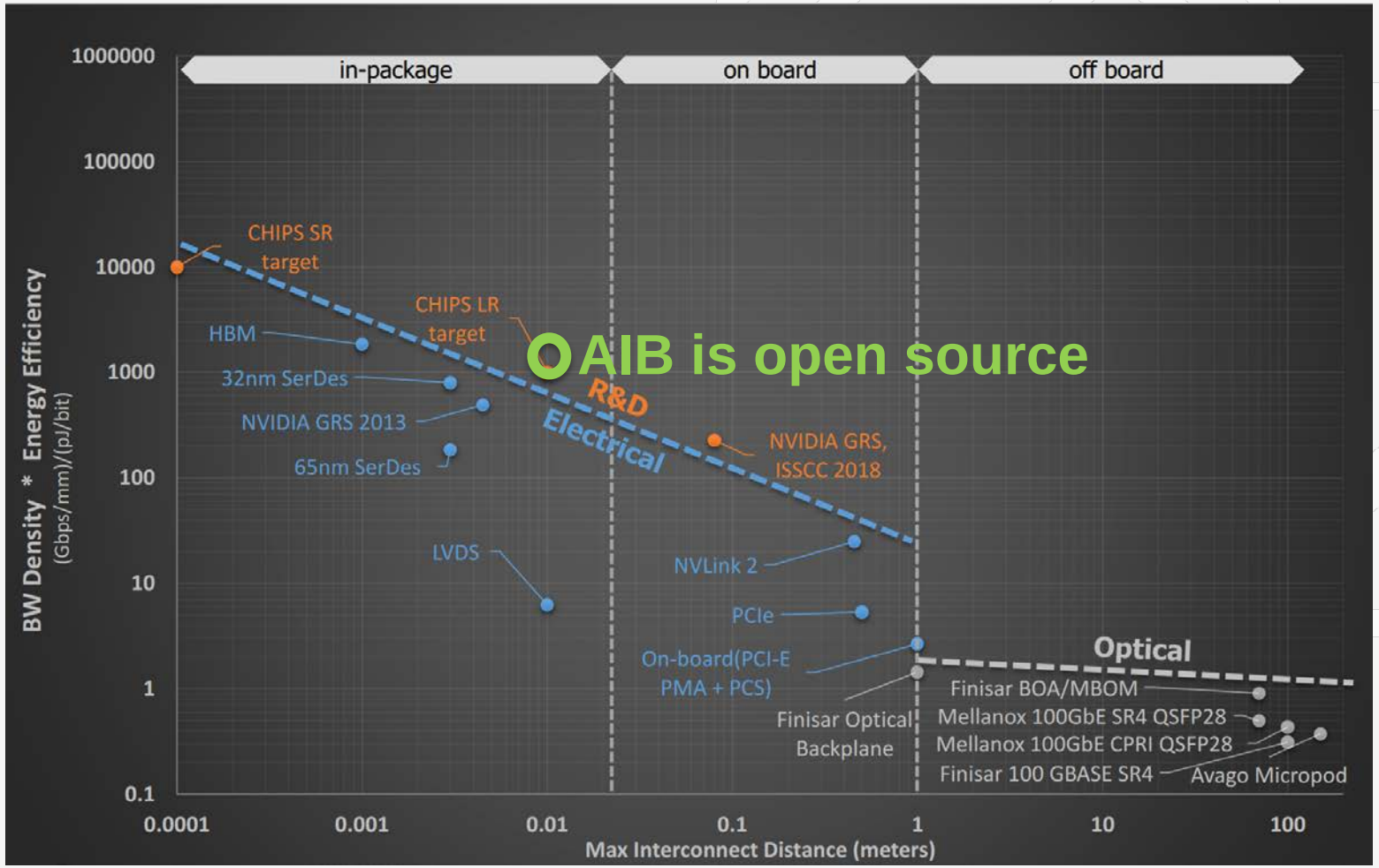


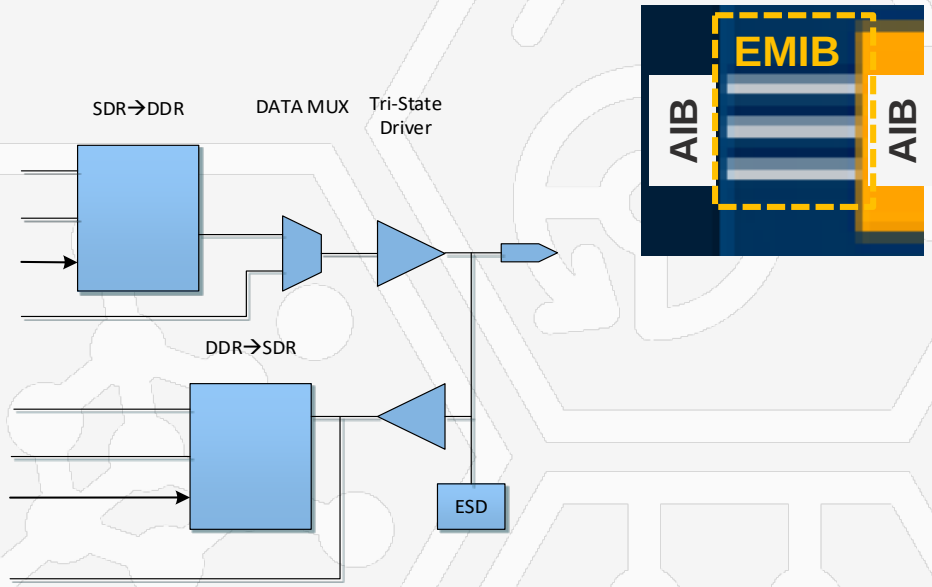


Intel® Embedded Multi-Die Interconnect Bridge (EMIB)

Platform for innovation through ecosystem
Explore new business models
Seeking to develop new partnerships

CHIPS: FOM & INTERFACE





AIB Configurable IO Cell

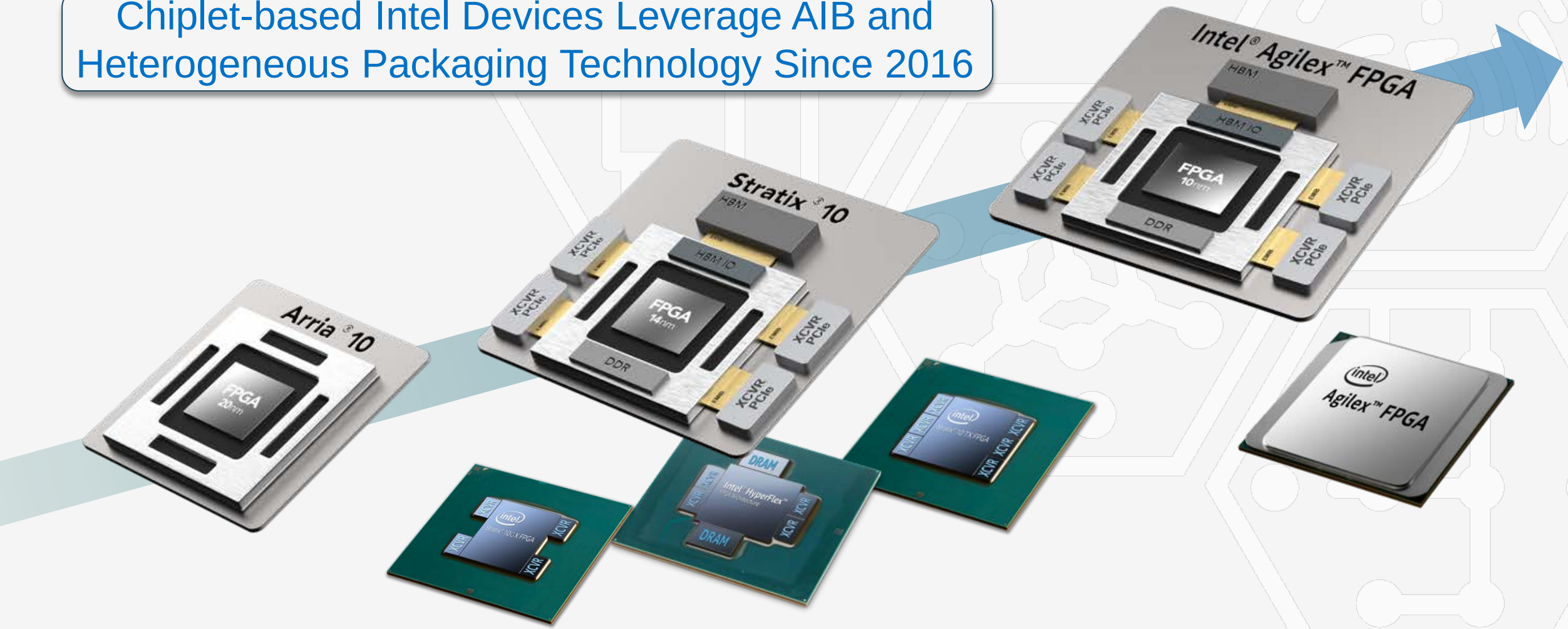
- Parallel in-package (2Gbps/IO)
- At ~3ns latency
- Over 1st gen EMIB (500 IOs/mm)
- At 0.85pJ/bit (for 55um ubump)

FOM = (2Gbpsx500/mm)/(0.85pJ/bit)=1176

Heterogeneous Integration with SoC-like performance

INTEL® FPGA EVOLUTION: HETEROGENEOUS IS HERE

Chiplet-based Intel Devices Leverage AIB and Heterogeneous Packaging Technology Since 2016



2014: Monolithic

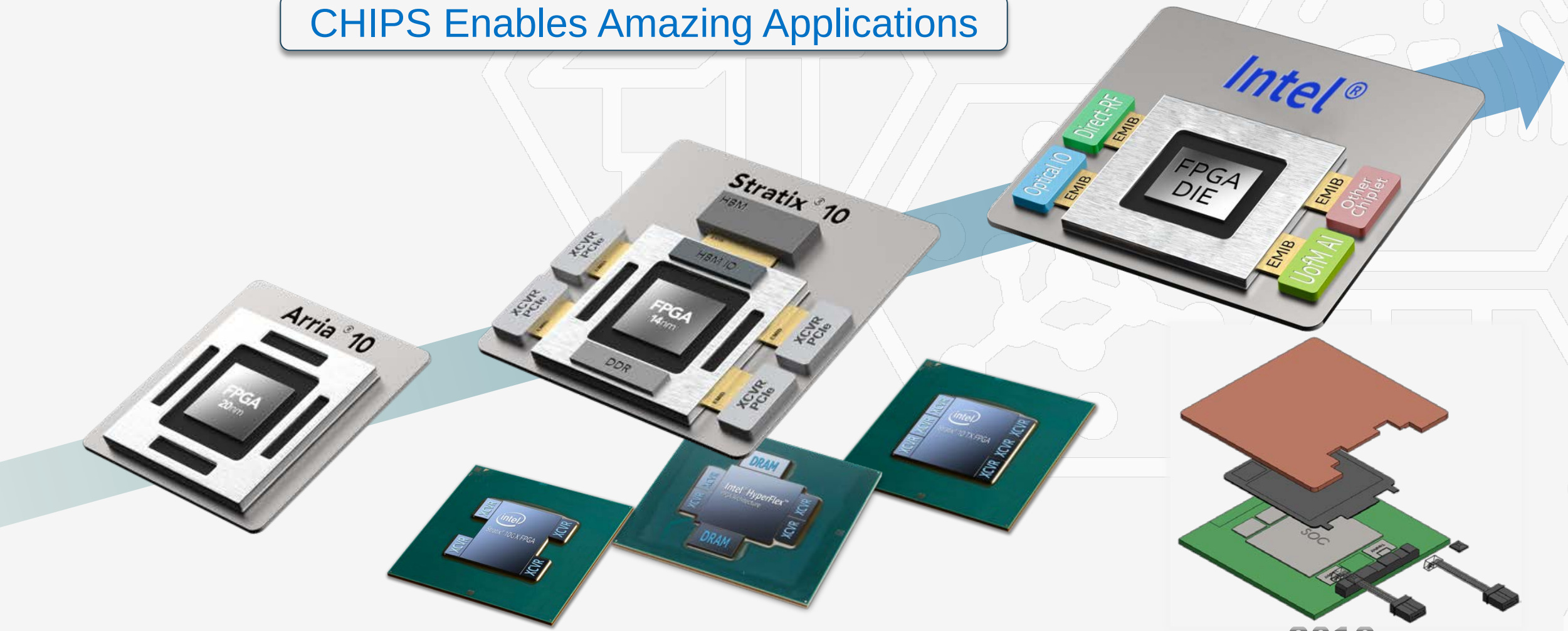
2016: 1st TRCV Chiplet

2017: 1st HBM, 2 TRCV nodes

2019: More Chiplets

INNOVATION VIA INTEGRATION: PARTNERSHIP

CHIPS Enables Amazing Applications



2014: Monolithic

2016: 1st TRCV Chiplet

2017: 1st HBM, 2 TRCV nodes

2019 RF to Photons Demonstration

CHIPS: REVOLUTIONARY SYSTEM INTEGRATION

Direct-RF

Uncompromised RF performance
(GOMAC 2019)

Optical IO

Breaking connectivity bottleneck
(HOTCHIPS 2019)

Research Platform

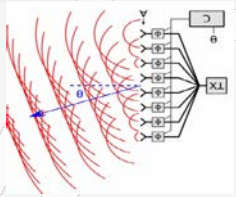
Research at commercial level
UofM AI Chiplet

Chiplet-Based Architecture

Library of chiplets: XCVR,
custom I/O & compute tiles

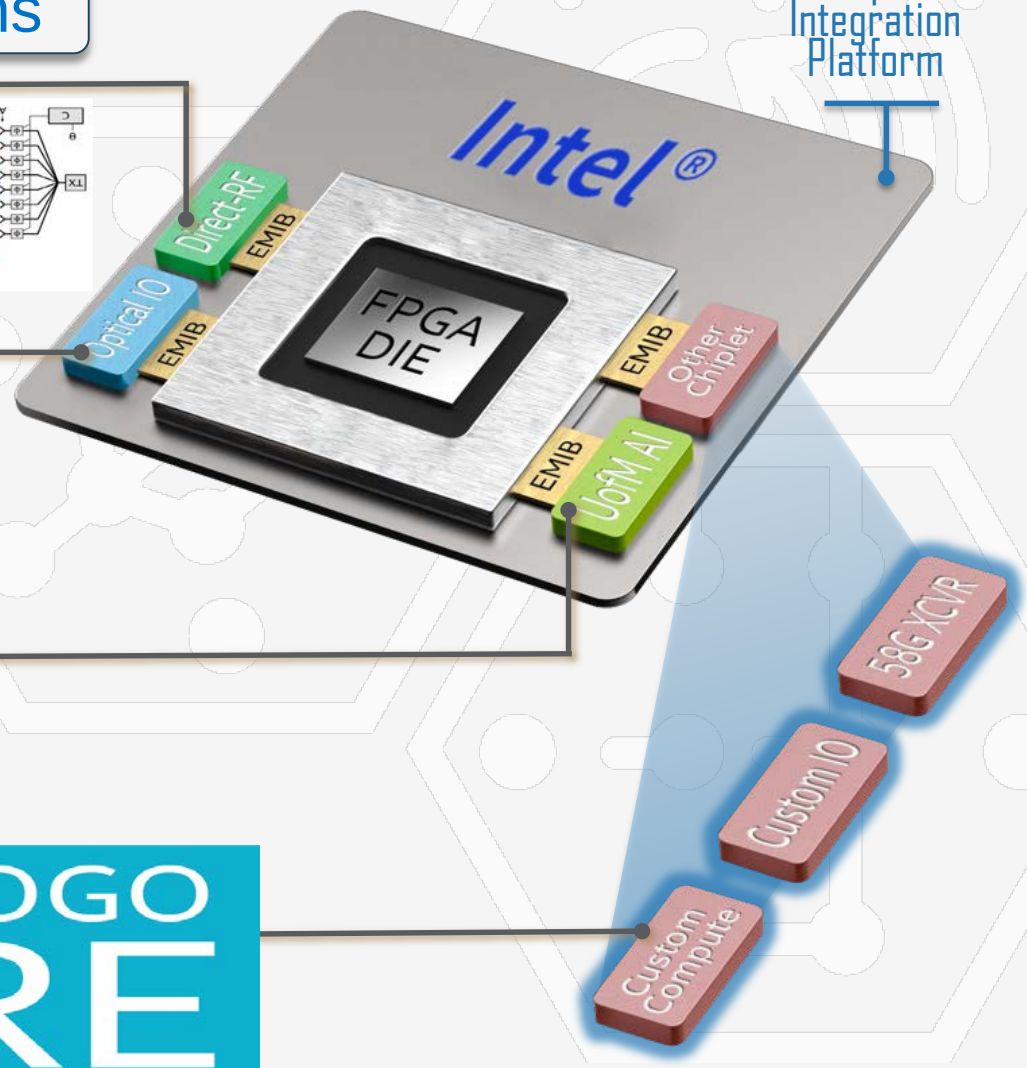
CHIPS Enables Amazing Applications

JARIET Technologies



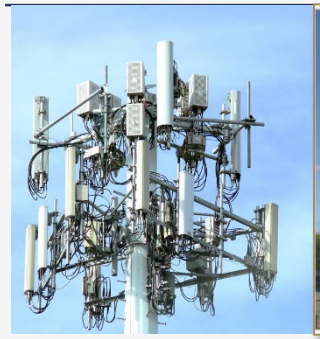
Ayar Labs

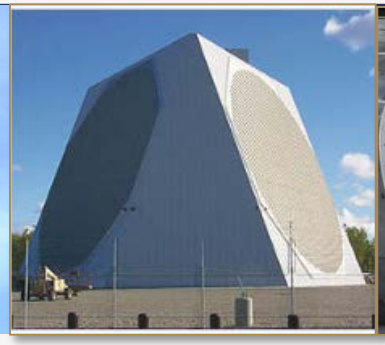
UNIVERSITY OF MICHIGAN

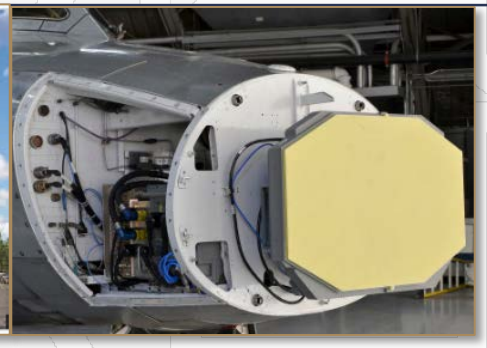


YOUR LOGO HERE

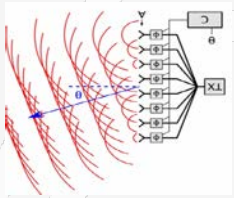
CHIPS: APPLICATION TO WIRELESS SYSTEMS

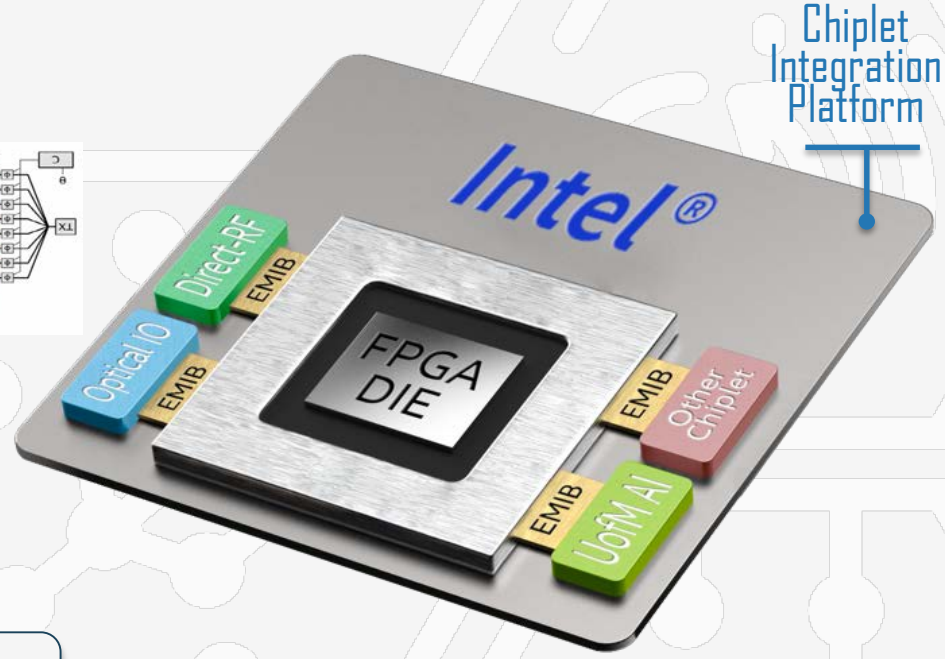






- **Systems Trending Towards All Digital**
- **Data Converters at Every Antenna**
- **Size, Weight and Power**





RF Integration Options

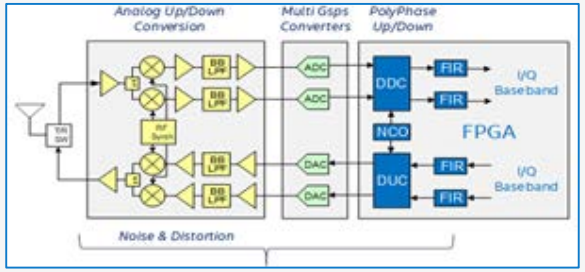
On Board (Discrete Analog Devices Connected via JESD)	Monolithic (Traditional SoC)	Chiplet (Chiplet Integration Platform, i.e. CHIPS)

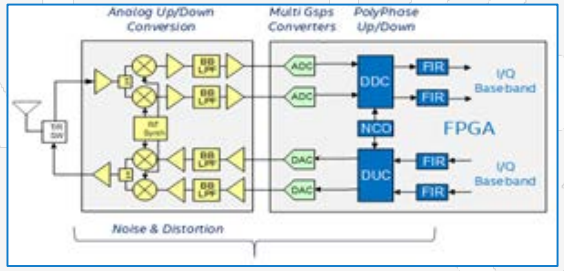
CHIPS: DIRECT-RF CHIPLET BENEFITS

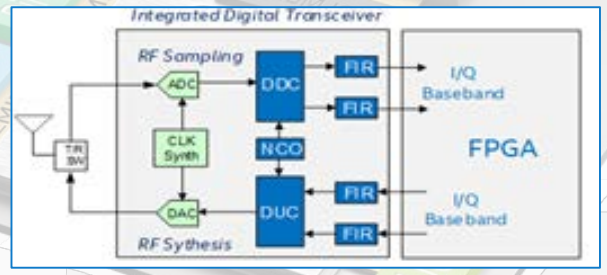
JARIET Technologies

intel

On Board: (Discrete Analog Devices Connected via JESD)	Monolithic (Traditional SoC)	Chiplet (Chiplet Integration Platform, i.e. CHIPS)







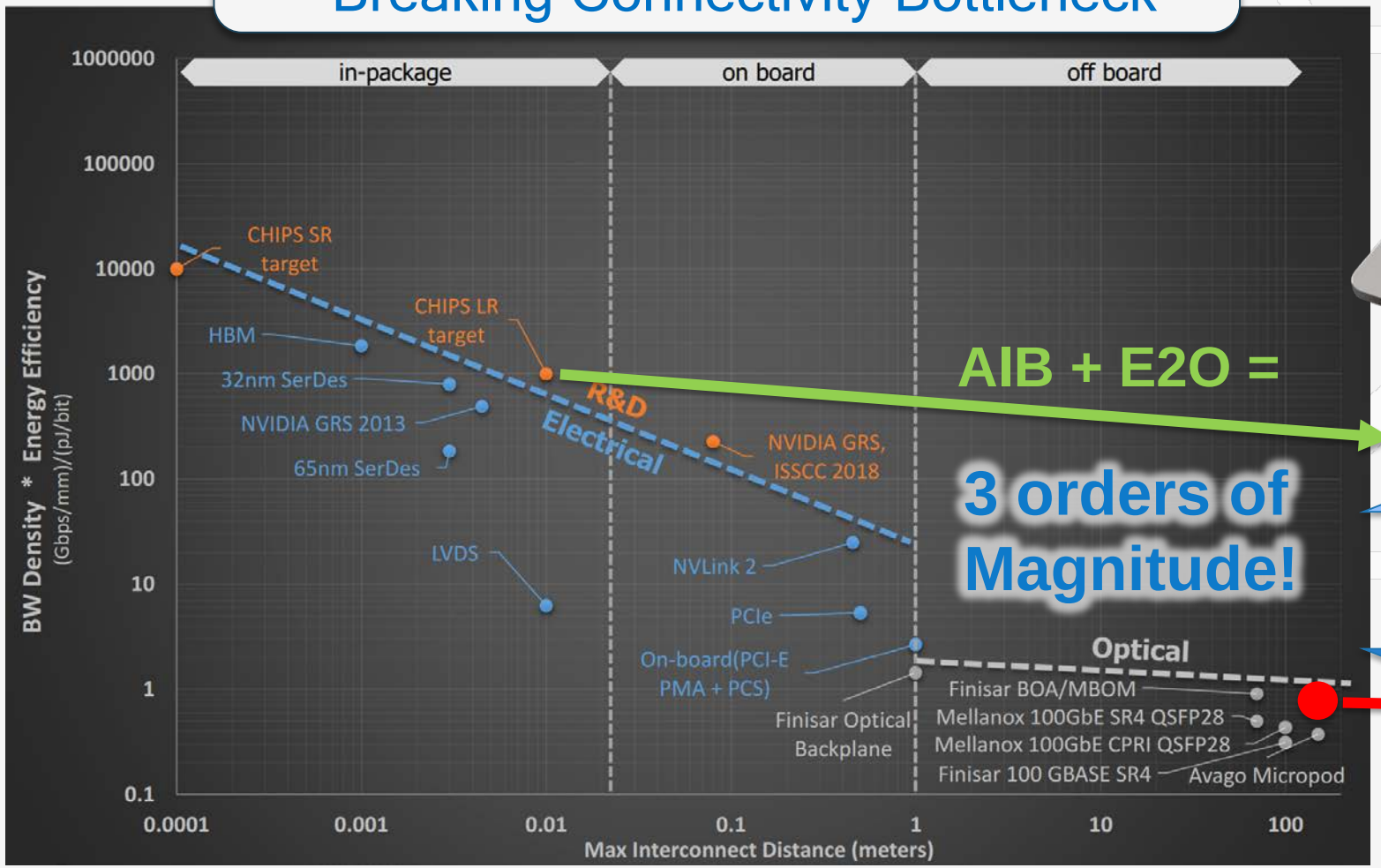
Parameter	Benefits of Chiplet Approach vs. Alternatives
Sample Rate: Up to 64 GSPs	~6x and higher sample rates, superior performance over higher BW
IBW: >25GHz	8x higher bandwidth
IF Stage	Not required, reducing SWAP, Improved system NF
JESD	No JESD Required, Reducing power

Opportunities to Improve Size, Weight and Power with Partner Innovation

CHIPS: OPTICAL IO CHIPLET BENEFITS

Ayar Labs intel

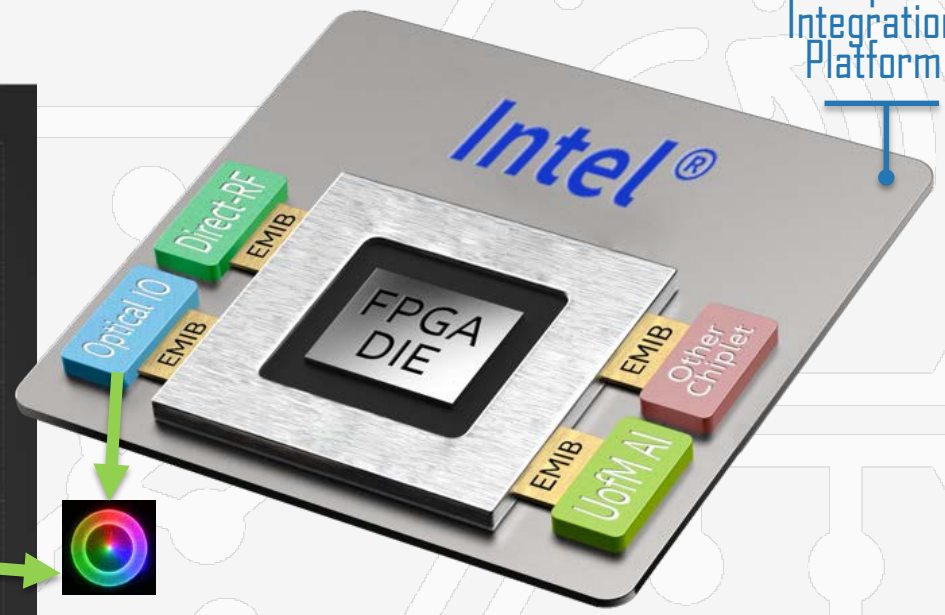
Innovate with Partners
Breaking Connectivity Bottleneck



AIB + E2O =

3 orders of Magnitude!

Chiplet Integration Platform



2011:
1st optical FPGA

SUMMARY

The Time for Chiplets Is Now

- Chiplets needed to drive joint innovation
- We have the technology
- Chiplet-based Intel Stratix 10 devices shipping since 2016

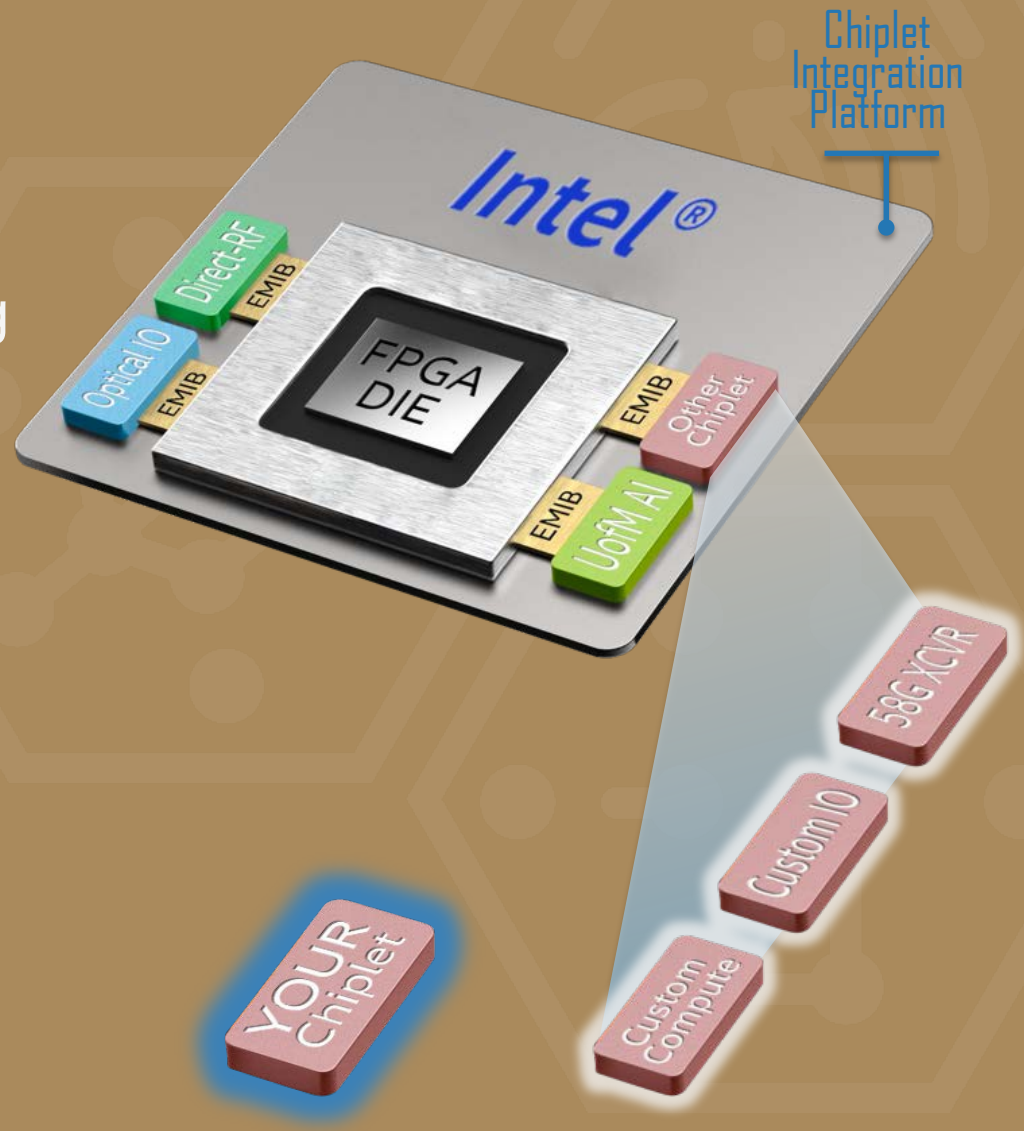
Significant Chiplet Milestones This Year

- Optical + DirectRF + University Research
- 2nd chiplet-based family (Intel Agilex FPGAs) begins shipping

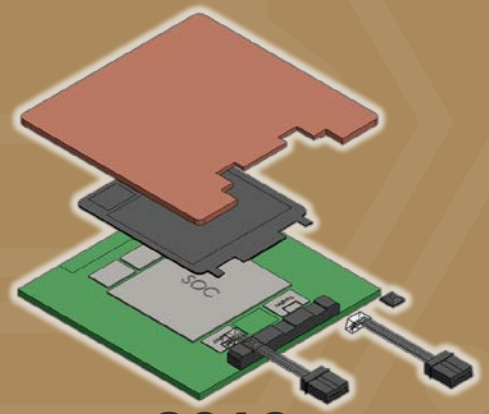
Join the Growing Chiplet Ecosystem

- Your chipet here!
- How can you leverage 1Tb/s of BW?

Start here for more information, specifications, and more: https://intel.ly/2LISZcr



ACKNOWLEDGMENT



2019

RF to Photons

The author would like to thank **Dr. William Chappell**, **Dr. Dan Green, Mr. Andreas Olofsson** and **Dr. Gordon Keeler** for their support.

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